VIDYA PRATISHTHAN'S KAMALNAYAN BAJAJ INSTITUTE OF ENGINEERING & TECHNOLOGY, BARAMATI

Department of Electronics & Telecommunication Engineering

Departmental Master Time Table 2026-27 SEM-I

(w.e.f - 29th June 2026)

Day	Time	9.15 To 10.15	10.15 To 11.15	11.15 To 11.30	11.30 To 12.30	12.30 To 01.30	1.30 To 2.45	02.45 To 03.45	03.45 To 04.45	04.45 To 05.45
	Class/ Period	1	2		3	4		5	6	7
Monday	S.Y.B.Tech	DLD-A (DE Lab) BHP S&S-B (SSD Lab) JSR(1Hr) AC-D (COMM LAB) SRS VSC-C (VLSI Lab) - RSP		SHORT RECESS	DLD - BHP (15)	S&S-JSR (15)	Lunch Break	Community Project C-SP Lab JSR VSC-D (VLSI Lab) RSP		HON-T1(15)
	T.Y.B.Tech	DSP-PNA (15)	ES&RTOS-VSS (15)		ES&RTOS-A (SSD Lab) VSS DSP-B (SP LAB) PNA FIP-D (VLSI Lab) SDB VSC C-(COMM Lab) MMJ			FIP-SDB(15)	MDM-R&A C-(CoE DMRA) -VCT EFT tut B,D-(VLSI Lab) RSP(4.30-5.30)	
	Final Year B.Tech									RM-SDB(14)
Tuesday	S.Y.B.Tech	DLD-B (DE Lab) BHP S&S-C (SSD Lab) JSR (1 Hr) AC-A (COMM LAB) SRS MDM DS-D SDL Lab IT SSP			AC - SRS (15)	DLD - BHP (15)		AEM-SSK (15)	Hon - (BFL Lab) T1	
	T.Y.B.Tech	HON-T1(15)	DSP-PNA (15)		FIP-A (VLSI Lab) SDB ES&RTOS-B (SSD Lab) VSS DSP-C (SP Lab) PNA VSC D -(COMM Lab) MMJ			ES&RTOS-VSS (14)	MDM-R&A B-(CoE DMRA) -VCT EFT tut A-(VLSI Lab) RSP (1hr) EFT tut C-(VLSI Lab) RSP (1hr)	
	Final Year B.Tech									ED-SDB(14)
Wednesday	S.Y.B.Tech	MDM DS-A SDL Lab IT SSP DLD-C (DE Lab) BHP S&S-D (SSD Lab) JSR(1 Hr) Comm. Project B-SP Lab SRS			S&S-JSR (15)	AC - SRS (15)		DLD - BHP (15)	AEM-SSK (15)	
	T.Y.B.Tech	FIP-SDB(15)	EFT-RSP(15)		ES&RTOS-C (SSD Lab) VSS FIP -B (VLSI Lab) SDB DSP-D (SP Lab) PNA VSC A -(COMM Lab) MMJ			DSP-PNA (14)	MDM R& A- MSY(14)	HON-T1 2 hrs (14)
	Final Year B.Tech									PSA-MSG(15)
Thursday	S.Y.B.Tech	AC-B (COMM LAB) SRS DLD-D (DE Lab) BHP S&S-A (SSD Lab) JSR (1hr)			AEM-SSK (15)	S&S-JSR (15)		AC - SRS (15)	MDM-DS-SSP (15)	VSC-RSP(15)
	T.Y.B.Tech	MDM R& A-MSY(15)	FIP-SDB(15)		ES&RTOS-D (SSD Lab) VSS FIP-C-(VLSI Lab) SDB DSP-A (SP Lab) PNA VSC B -(RMT Lab) BHP			EFT-RSP(14)	VSC-BHP(14)	Hon - (SSD Lab) T1 2 hrs
	Final Year B.Tech									
Friday	S.Y.B.Tech	HON-T1(14)	MDM-DS-SSP (14)		VSC-A (VLSI Lab) - RSP MDM DS-B SDL Lab IT SSP AC-C (COMM LAB) SRS Comm. Project D-SP Lab Dixit			Comm. Project A -SP Lab JSR VSC-B (VLSI Lab) RSP MDM DS-C SDL Lab IT SSP		
	T.Y.B.Tech	ES&RTOS-VSS (15)	MDM R& A-MSY(15)		MDM-R&A A (CoE DMRA) -MSY			MDM-R&A-D (CoE DMRA) -MSY		AC-Col-RSP(15)
	Final Year B.Tech									

Time-Table In-Charge
R.S Piske

Time-Table Co-ordinator
Dr D G Patil

HoD
Dr J S Rangole

Principal
Dr S B Lande

S.Y.B.Tech
AEM :-Advanced Mathematics for E&TC Engineering- S.S.Khot
AC:-Analog Circuits :- S.R.Sabale
DLD:- Digital Logic Design -: Dr. B.H. Patil
S&S:Signal &System :- Dr. J.S.Rangole
VSC: Programming in Python-: R.S.Piske
MDM DS :-Multidisciplinary Minor Course-Data Structures:- Devika Mehta
HON- Honor -T1
CP:Community Project:-All Faculties

T.Y.B.Tech
ES&RTOS:-Embedded System & RTOS :- V.S.Surwase
DSP-Digital Signal Processing :-Dr.P.N.Arotale
PEL-I(FIP)Fundamentals of Image Processing:Mr.S.D.Biradar
MDM :-Multidisciplinary Minor Course-:- Robotics and Automation: Mona S Yadav/Dr. V.C.Todkari
AC: Audit Course: R.S.Piske
Electromagnetic Field Theory:- R.S.Piske
Vocational Skill Course: MMJ/BHP/PPG
HON- Honor System Verilog For Design AndVerification -T1

Final Year.B.Tech
ED:Entrepreneurship development: S.D. biradar
RM: Research methodology:- S.D. Biradar
PSA: Public speaking and aptitude: M.S.Gawade